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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,037	07/13/2001	Zine Eddine Boutaghou	STL 9721	2226
7590 01/09/2006			EXAMINER	
Seagate Technology LLC Intellectual Property Department 7801 Computer Avenue South-NRW097 Bloomington, MN 55435			VINH, LAN	
			ART UNIT	PAPER NUMBER
			1765	
DATE MAILED: 01/09/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/905,037	Applicant(s) BOUTAGHOU, ZINE EDDINE	
	Examiner Lan Vinh	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 31-50 is/are pending in the application.
- 4a) Of the above claim(s) 39-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 31-38 and 43-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species V (claims 31-38, 43-49) in the reply filed on 12/22/2005 is acknowledged.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 46-49 been renumbered 47-50..

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 31-38, 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Bulat et al (US 5,192,699)

Bulat discloses a method for fabricating FET semiconductor device. The method comprises the steps of:

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positioning a photoresist layer 32/mask relative to a semiconductor structure/device, the layer 32/mask being formed of a pattern exposing a surface of the semiconductor structure/device (col 4, lines 30-32; fig. 8)

etching the patterned layer 32 into a surface of the structure to form a etched layer/feature, the feature includes one rounded edge/bending/arcuate edge (col 4, lines 52-64; figs 9-10)

providing a contact member 35B connected to the feature (col 5, lines 9-15; fig. 12), which reads on providing a mating element and connecting the mating element and the feature

Regarding claim 32, Fig. 10 of Bulat shows that the etched layer/feature is formed into the substrate

Regarding claim 34, Fig. 10 also shows that etched layer/feature protrudes from the substrate

Regarding claims 37-38, Figs 8-9 show the patterned mask 32 is form with variable spacing to produce the rounded slope and varied rounded slopes, the mask is formed with spacing that are closer near the surface of the device and more widely spaced near the sidewall

The limitations of claims 33, 35, 36 have been discussed above

Regarding claim 44, Balut discloses that the semiconductor structure comprises a layer 30, the layer 30 is being etched (col 4, lines 59-65)

Claim Rejections - 35 USC § 103

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5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over in Bulat et al (US 5,192,699) view of Berry et al (US 6,344,383)

Bulat method has been described above. Bulat differs from the instant claimed invention as per claim 43 by performing RIE etching instead of ion beam etching

Berry, in a method for manufacturing semiconductor, discloses dry etching using plasma etching or ion beam etching (col 6, lines 22-25)

One skilled in the art at the time the invention was made would have found it obvious to modify Bulat method by using ion beam etching instead of RIE etching in view of Berry teaching because Berry discloses that reactive ion etching (RIE) and ion beam etching are standard dry etching techniques in the art (col 6, lines 20-23)

7. Claims 45-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over in Bulat et al (US 5,192,699) view of Wada et al (US 5,001,080)

Bulat discloses a method for fabricating a semiconductor device. The method comprises the steps of:

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etching a patterned layer 32 into a surface of a semiconductor device to form an etched layer/feature, the feature includes one rounded edge/bending/arcuate edge (col 4, lines 52-64; figs 9-10)

providing a contact member 35B connected to the feature (col 5, lines 9-15; fig. 12), which reads on providing a mating element and inserting the mating element into the feature. Bulat also discloses that the rounded edges eliminate abrupt steps in the structure, thus assuring that the deposited metal contacts and connections are of adequate thickness throughout (col 5, lines 38-44), which reads on the rounded edge reduces damage to the feature

Unlike the instant claimed invention as per claim 45, Balut fails to disclose that the semiconductor device is a MEMS device

Peterson discloses a method for protecting a microelectronic (MEMS) using a rounded patterned masking layer 14 (col 7, lines 22-27, fig 1C)

Since both Balut and Peterson are concerned with a method using rounded patterned masking layer, one skilled in the art would have found it obvious to employ Balut's rounded masking layer on a MEMS device in view of Peterson teaching because Peterson discloses that the MEMS elements are stabilized and protected by protective coating 14/rounded masking layer (col 8, lines 41-44)

Regarding claim 46, Fig. 10 of Bulat shows that the etched layer/feature is formed into the substrate

Regarding claim 48, Fig. 10 also shows that etched layer/feature protrudes from the substrate

The limitations of claims 47, 49-50 have been discussed above

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Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LV

January 3, 2006